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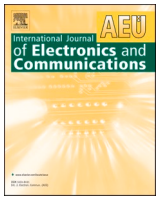

Regular paper

Compact low-loss diplexer with stacked 2D and 3D structures using 3D glass-based advanced packaging technology

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ABSTRACT

A compact low loss wideband diplexer is introduced by using stacked 2D and 3D structures through 3D advanced packaging and through glass vias (TGV). An inductor is designed by using stacked 2D and 3D structures to reduce the coupling effect between adjacent 2D inductors located in the same layer. It can greatly improve the Q factor yet minimize the chip size. This low loss, small size diplexer is developed by virtue of a modified topology and the proposed stacked 2D and 3D structures. The designed diplexer with a compact size of 1.6 mm × 0.8 mm × 0.25 mm is fabricated using 3D glass-based advanced packaging technology and measured by on-wafer probing. The measured results indicate that it achieves an insertion loss less than 0.8 dB and 0.9 dB and an isolation better than 20 dB and 17.5 dB in the bands of 0.699 GHz-0.960 GHz and 1.71 GHz-2.69 GHz, respectively. In comparison with the previously reported designs, the proposed diplexer shows the superior advantages of smaller size and lower insertion loss.

1. Introduction

Filtering diplexers with low insertion loss, high isolation and miniaturized size play significant roles in RF systems. Designing diplexers with good performance are critical and challenging for dual band applications in 3G and 4G bands, which are attractive choices for RF systems and wireless communication systems nowadays.

In recent years, many diplexer design methods have been proposed, including electric and magnetic coupling [1–3], mixed multimode resonators [4–6], electromagnetic perturbation technology [7], metal strip line resonators [8], releasable filling structure technique [9], and so on. In [1], the diplexer was designed by virtue of coupling, which can achieve a high-isolation and wide-stopband performance. However, its insertion loss is 2.3 dB, which is too large for the applications in wireless communication systems. In [4], the diplexer was designed by using multimode, which achieved an insertion loss of 1.3 dB. However, its circuit size is 33.6 mm × 23.4 mm, which is too large for integration and packaging. In [8], the diplexer with an insertion loss of 1.0 dB was developed, which meets the loss criterion of RF systems. However, the diplexer is working at 85.6 GHz and 94.5 GHz, which is out of 3G, 4G, 5G and sub-6G bands. To obtain the diplexers working at the lower bands with low insertion loss, some designs have been reported [10–14]. In [10], a diplexer working at 2.4 GHz – 2.5 GHz and 5.15 GHz – 5.85 GHz bands were reported with insertion losses less than 1.67 dB and 1.58 dB, respectively. However, the device size of 14.6 mm × 10.48 mm is too large. And in [11], a (2.4 GHz WLAN/3.5 GHz WiMax) diplexer with a size of 23.8 mm × 11.5 mm is designed, which is not suit for integration. In [12], a diplexer was reported with an insertion loss less than 0.41 dB, but its size is also too large. There are some compromises among small size, low insertion loss, and working frequency in the above diplexer designs. Besides, to achieve the high-isolation performance, some coupling methods have been introduced in the designs reported [1–3], but the insertion loss and size are always too large. And some novel structures [14–19] with high Q

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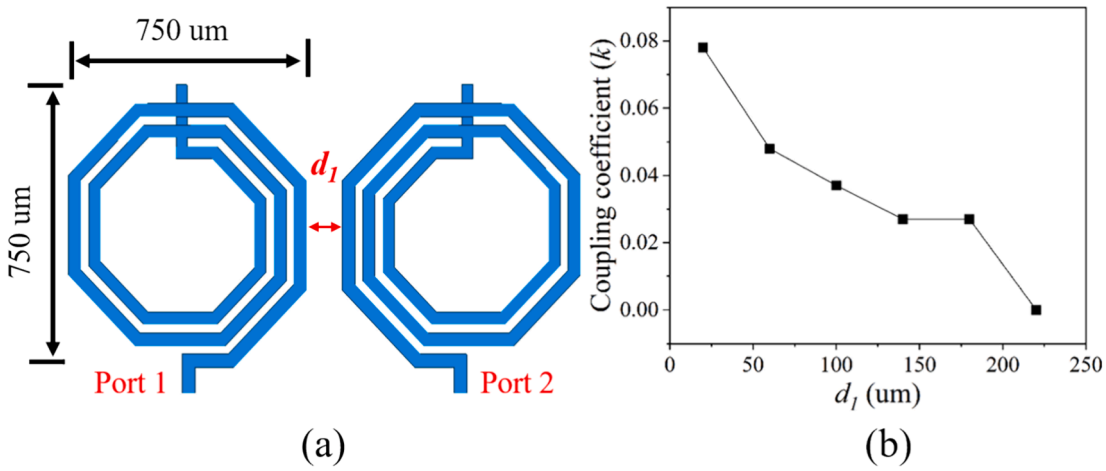

Fig. 1. (a) The structure of the planar 2D inductors. (b) Simulated coupling coefficient results of the two plannar 2D inductors.

factor are reported to reduce the loss, but the size is also too large to be integrated. Therefore, to obtain the small size and low insertion loss, a stacked 2D and 3D structures with no coupling is proposed here.

In this work, a compact and low-loss diplexer working at the 3G and 4G bands is developed using a 3D glassed-based advanced packaging technology. This diplexer consists of stacked multiple 2D and 3D structures to resolve the compromising issue between low insertion loss and small size. The low loss can be obtained by using high-Q 3D inductor, whereas the small-size is achieved by stacking 2D inductor and 3D-inductor together, which can reduce the coupling effect between adjacent 2D inductors located in the same layer. Moreover, a modified topology is introduced in this diplexer, which can achieve a good low-pass and bandpass performance and generate three transmission zeros outside each operating band for high out-of-band rejections. The designed diplexer by virtue of a modified topology and the proposed stacked 2D and 3D structures has a size of 1.6 mm × 0.8 mm × 0.25 mm and achieves an insertion loss less than 0.8 dB and 0.9 dB and an isolation better than 20 dB and 17.5 dB in the bands of 0.699 GHz-0.960 GHz (the fractional bandwidths is 31.46 %) and 1.71 GHz-2.69 GHz (the fractional bandwidths is 44.55 %), respectively.

2. Proposed diplexer design

2.1. Stacked 2D planar inductor and 3D inductor

It is well known that the inductors placed on the same layer can generate strong coupling, which not only affects the performance of individual inductors but also is hardly handled during optimization. The inductors could be placed far apart to reduce the coupling. However, it enlarges the chip size. It is highly desirable to reduce unnecessary coupling effects yet achieve size miniaturization. Fig. 1a shows two identical 2D planar inductors, which have a size of 750 μm × 750 μm and an inner radius of 300 μm, placed in the same layer. The distance of the two planar 2D inductors is denoted as d_1. Port 1 and port 2 are defined at an end of each 2D inductor, as shown in Fig. 1a. To study the coupling effect, the S-Parameter is computed when distance d_1 increases from 20 μm to 220 μm with a step size of 40 μm. The coupling coefficient k can be determined as [1]

$$k = \frac{f_{02}^2 - f_{01}^2}{f_{02}^2 + f_{01}^2} \tag{1}$$

where f_{01} and f_{02} are the frequencies of two transmission poles. Fig. 1b depicts the coupling coefficient versus d_1. When the d_1 is greater than 220 μm, as shown in Fig. 1b, the coupling between adjacent 2D planar inductors is negligible. Therefore, to reduce the coupling effect between adjacent 2D planar inductors, it is necessary to increase the distance d_1, which is, however, not conducive to the size miniaturization.

To solve the issue above, a new design with stacked 2D planar inductor and 3D inductor is herein introduced. Fig. 2a shows the stacked planar 2D inductor and 3D inductor on the 3D glassed-based advanced packaging technology. The 3D inductor is constructed in the BM1, TGV and M1 layers, whereas the 2D inductor is constructed in the M2 layer. The MIM capacitors are located at the M1, VIA and M2 layers. The thicknesses of the BM1, TGV, M1, VIA and M2 layers are 5 μm, 230 μm, 5 μm, 5 μm and 5 μm, respectively. The 2D inductor is located on the top layer (M2), whereas the 3D inductor is located on the bottom layers (BM1, TGV and M1), as shown in Fig. 2b. The 2D inductor occupies a size of 750 μm × 750 μm with an inner radius of 300 μm, while the 3D inductor occupies a size of 800 μm × 700 μm. The distance from the center of the 2D inductor to the edge of the 3D inductor is defined as d_2, which increases from 0 μm to 1000 μm with a spacing of 200 μm. When $d_2 = 800$ μm, there is no stacking area between the 2D inductor and the 3D inductor.

The magnetic field distributions of 2D planar inductor and 3D inductor are shown in Fig. 2c and 2d, respectively. Since the current loops in the stacked 2D planar inductor and 3D inductor are virtually orthogonal each other, it can be inferred from the magnetic field perspective that there is almost no coupling between them. It can be concluded that the coupling coefficient k is almost zero regardless how close the stacked 2D planar inductor and 3D inductor could be. Therefore, this design with stacked 2D planar inductor and 3D inductor can greatly miniaturize the design size. In addition, since the 3D inductor has a higher Q factor than the pure 2D planar inductor of the same area size [14], the simulated inductance and Q factor of the 2D planar inductor and high-Q 3D inductor with the similar dimension of

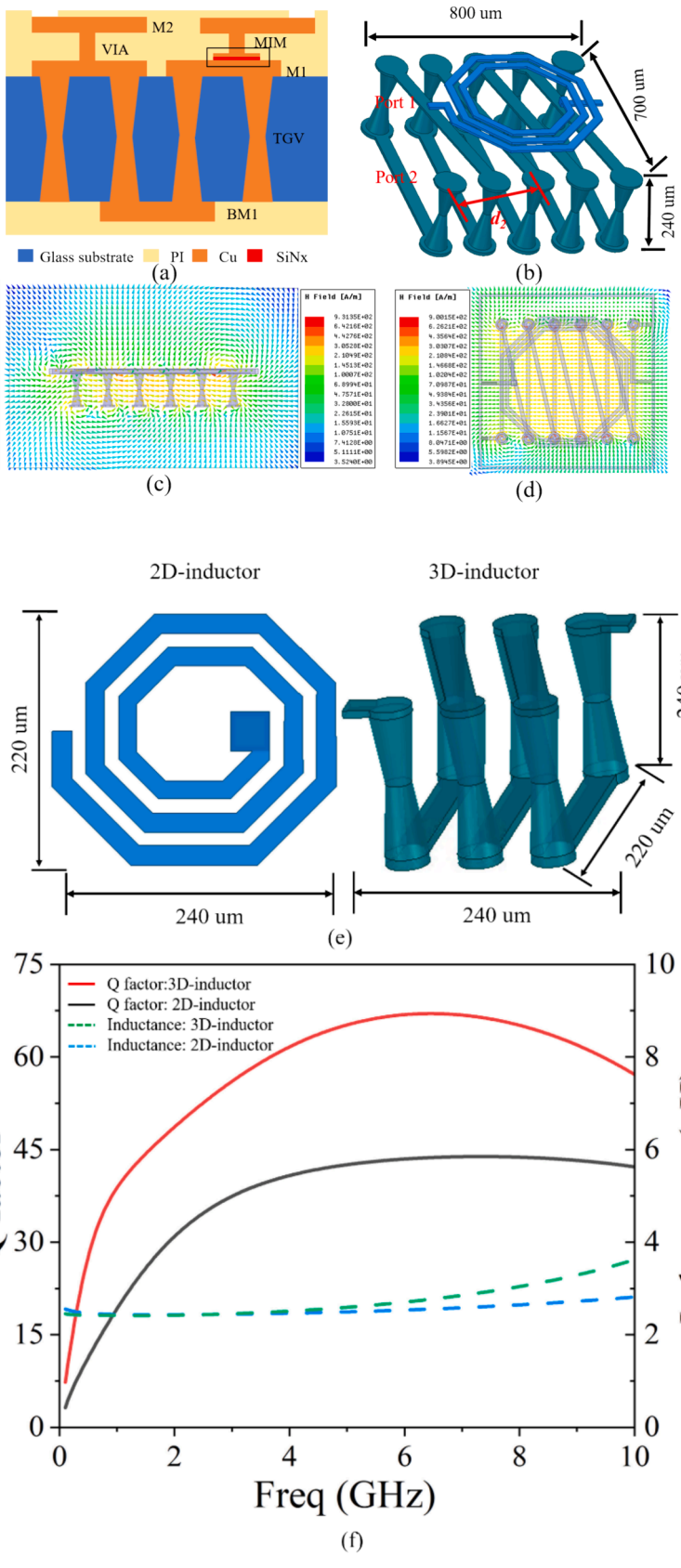

Fig. 2. (a) Cross-section of glass-based 3D packaging technology. (b) Stacked 2D and 3D inductors. (c) Magnetic field distributions of 2D planar inductor. (d) Magnetic field distributions of 3D inductor. (e) The structure of the 2D inductor and 3D inductor. (f) The Q factor and Inductance of the 2D inductor and 3D inductor.

240 μm × 220 μm are compared in Fig. 2e and 2f. It shows the Q factor (about 35 ~ 50 in operating bands) of this 3D inductor is also twice as high as that of the 2D planar inductor, while the inductances of both inductors are similar in the operating frequency range 0.699–0.96 GHz and 1.71–2.69 GHz. Therefore, the solution of using high-Q 3D inductor can reduce the insertion loss of the designed filter. Then this design with stacked 2D planar inductor and 3D inductor not only miniaturizes the design size, but also achieves high Q and reduces the insertion loss.

2.2. Proposed diplexer

The 3D layout of a proposed diplexer using multiple copies of stacked 2D planar inductor and 3D inductor is shown in Fig. 3a. And the 3D layout is modeled by UltraEM [20], it is composed of a low-pass filter and a band-pass filter. The proposed diplexer has a miniatured size of 1.6 mm × 0.8 mm × 0.25 mm and is fabricated in the 3D glass-based advanced packaging technology. In Fig. 3a, L1 and L4 are 2D inductors, while L_2 and L_3 are 3D inductors. Moreover, L_1 and L_2 form a design of stacked 2D and 3D inductors, whereas L_3 and L_4 form another design of stacked 2D and 3D inductors. As shown in Fig. 3a, multiple copies of stacked 2D and 3D inductors can make the diplexer design much more compact.

Fig. 3b illustrates the equivalent circuit of the proposed diplexer and the simulated results of the circuit is shown in Fig. 3c. And the insertion loss less than 0.7 dB and 0.8 dB, the return loss better than 17 dB and 15 dB, and the isolation better than 23 dB and 20 dB in the operating bands. The modified topology simulated by the FDSPICE [21] is introduced in this diplexer, which can achieve a good low-pass and band-pass performance and generate three transmission zeros outside each operating band for high out-of-band rejections. To analyze the low-pass circuit, because these two port networks are reciprocal, $Z_{21} = Z_{12}$, and the Z parameters can be written as

$$Z_{12} = Z_{21} = \frac{j(1-\omega^2 L_1C_1)(1-\omega^2 L_2C_2)}{-\omega[C_3(1-\omega^2 L_2C_2)(1-\omega^2 L_1C_1)-\omega^2 C_1C_3L_2+C_1(1-\omega^2 L_2C_2)]} \quad (2)$$

where ω is the frequency. The corresponding S parameters can be obtained as

$$S_{12} = \frac{2Z_{12}Z_0}{\Delta Z} \quad (3)$$

Once the frequency of $S_{12} = 0$ is determined, the transmission zeros frequency ω can be calculated as

$$\omega_1 = \sqrt{\frac{1}{L_1C_1}}, \omega_2 = \sqrt{\frac{1}{L_2C_2}} \quad (4)$$

herein, it is assumed that $C_1 = 0.79$ pF, $C_2 = 1.01$ pF, $C_3 = 4.35$ pF, and $L_1 = 1.39$ nH, and $L_2 = 6.97$ nH. Based on (2), it can be found that the two transmission zeros of the low-pass filter are located at 4.75 GHz and 1.9 GHz. Moreover, in order to analyze the band-pass circuit, and these two port networks are reciprocal, the Y parameters can be written as

$$Y_{12} = Y_{21} = -\frac{j\omega C_4C_5(1-\omega^2 L_3C_6)(1-\omega^2 L_4C_7)}{C_6+C_4(1-\omega^2 L_3C_6)(1-\omega^2 L_4C_7-\omega^2 L_4C_5)+C_5(1-\omega^2 L_3C_6)(1-\omega^2 L_4C_7)} \quad (5)$$

The corresponding S parameters can be obtained as

$$S_{12} = \frac{-2Y_{12}Y_0}{\Delta Y} \quad (6)$$

the transmission zeros frequencies ω_3 and ω_4 can be calculated as

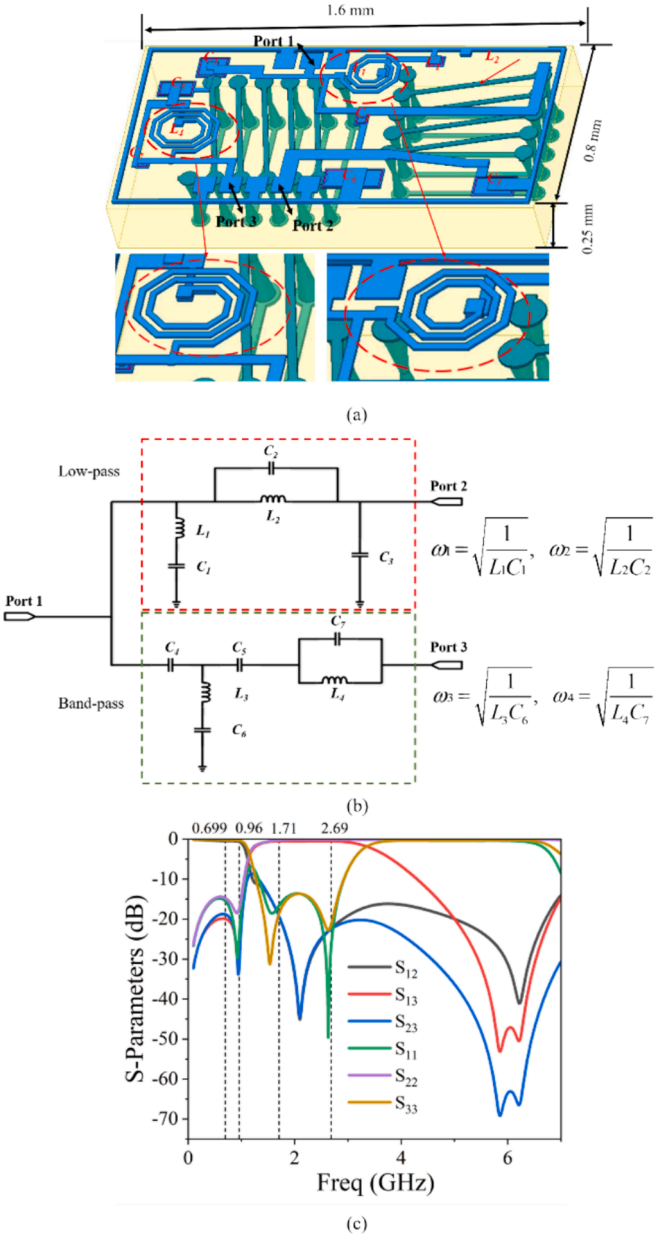

Fig. 3. Proposed diplexer. (a) 3D layout; (b) Equivalent circuit; (c) the simulated results of the equivalent circuit.

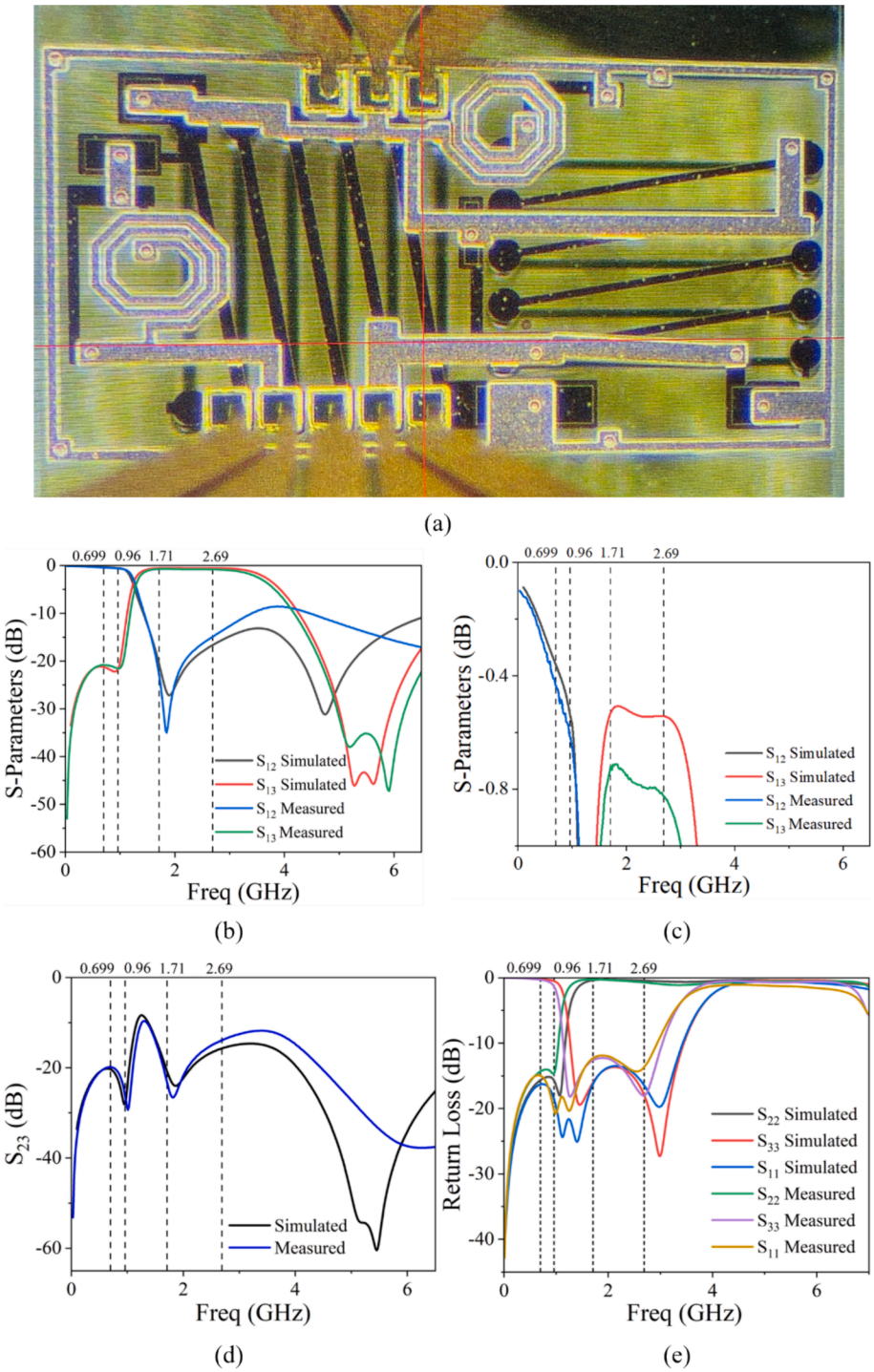

Fig. 4. (a) Micrograph of the proposed diplexer. (b) Simulated and measured S parameters of the proposed diplexer. (c) the enlarged images of the two-passband insertion loss in (b). (d) Simulated and measured isolations of the proposed diplexer. (e) Simulated and measured Return loss of the proposed diplexer.

$$\omega_3 = \sqrt{\frac{1}{L_3C_6}},\ \omega_4 = \sqrt{\frac{1}{L_4C_7}} \tag{7}$$

Herein, it is assumed that $C_4 = 3.35$ pF, $C_5 = 8.75$ pF, $C_6 = 8.52$ pF, $C_7 = 0.13$ pF, $L_3 = 3.93$ nH, and $L_4 = 6.51$ nH. Based on (5), it can be shown that the two transmission zeros of the band-pass filter are located at 0.9 GHz and 5.28 GHz. By combining the band-pass and low-pass filters into a diplexer, there are some influences caused by the parasitic parameters. Therefore, an additional transmission zero may be generated outside each of the two passbands, which are located at 1.1 GHz and 5. 8 GHz, respectively. The out of band transmission zero of the low-pass filter can be controlled by adjusting the values of L_1, C_1, L_2, and C_2, and by adjusting the values of L_3, C_6, L_4, and C_7, the transmission zeros of the band-pass filter can be controlled. Therefore, the proposed diplexer can achieve high selectivity and operate in different frequency bands.

And to directly obtain the dimensions of the inductors and capacitors, the EM simulation have been carried out. Since the capacitance can be defined as $C = \frac{\varepsilon_0 \varepsilon_r S}{d}$, where C represents capacitance (Farad), $\varepsilon 0$ is the dielectric constant in vacuum (approximately 8.854187817 × 10ˆ−12F/

Table 1
Performance of the proposed diplexer versus other diplexers.

Ref.	f_0 (GHz)	Insertion Loss (dB)	Size (mm^2)	Return Loss (dB)	Fractional Bands (in percentage)	Isolation (dB)	Technology
[4]	12/14	1.34/1.41	33.6 × 23.4	20/16	3.25 %/3.75 %	27/27	SIW
[5]	5.05/7.46	0.91/2.03	33.3 × 33.3	18/15	14.6 %/6.2 %	55/49	Folded-HMSIW
[10]	2. 5/5.55	1.67/1.58	14.6 × 10.48	12.5/12.5	26.94 %/27.45 %	26/26	Lumped element
[12]	1.8/2.4	0.41/0.41	11.9 × 7.4	12/10	3.83 %/3.79 %	39/39	High-temperature superconducting (HTS)
[15]	2.44/5.45	0.4/0.8	2.0 × 2.0	20/20	32.78 %/12.84 %	20/20	TGV-based
This work	0.8295/2.2	0.8/0.9	1.6 × 0.8	15/13	31.46 %/44.55 %	22/17.5	TGV-based

m), ε_r is the relative dielectric constant of the medium, S is the area of parallel plates (square meters), and d is the distance between parallel plates (meters). In the TGV-based technology we used, C can be calculated, $\varepsilon_r = 6.0$, and $d = 0.2$ μm, so the S can be obtained and the size of the capacitors can be obtained. However, the inductance can be calculated by the formula (2) and (5), and to achieve these inductances, the expression *im(1/Y(1,1))/(2*pi*freq) *1e9* were used into the EM simulation. By achieving the same calculated inductance values as the ones in electromagnetic simulation, the exact dimensions of the inductors can be obtained in electromagnetic simulation software. And then the final dimensions of the designed diplexer can be achieved.

3. Measurement

The proposed diplexer is simulated and designed by the full-wave electromagnetic simulator, UltraEM, from Faraday Dynamics [16]. The micrograph of the fabricated TGV-based diplexer is shown in Fig. 4a. The layout size of the fabricated BPF chip is 1.6 mm × 0.8 mm × 0.25 mm. Due to the influence of parasitic parameters, compared with the circuit level simulation results, the out of band of the low-pass filter in the electromagnetic level simulation is missing one transmission zero. The electromagnetic simulated and measurement results of the proposed diplexer are compared from Fig. 4b to Fig. 4e. The good agreement between the simulated and measured results is observed. The fabricated diplexer is measured on-chip using the Keysight N5244A PNA-X vector network analyzer and Cascade summit-11000 probe station. We applied the SOLT de-embedding method during the measurement process which is based on a 12-item error model and can reduce the impact of system errors on the measurement results. And we set the frequency step size very small about 10 MHz during the process of measurement. Therefore, the measured curves are smooth. However, compared with the simulated results, the measured results have a slight frequency shifted in the upper band due to the fabrication tolerance. And from the measured results, this design can achieve an insertion loss less than 0.8 dB and 0.9 dB, the return loss better than 15 dB and 13 dB, and an isolation better than 20 dB and 17.5 dB within the operation bands of 0.699 GHz-0.960 GHz and 1.71 GHz-2.69 GHz, respectively.

Table I summarizes the performance of the proposed diplexer. It is observed that the proposed diplexer can achieve a compact size (in relative to the maximum wavelength) by comparison with other designs. The proposed diplexer has lower insertion loss than those from [4] and [10]. And compared with [15] based on the same technology, the proposed one worked at the lower bands and has the miniaturized size. Moreover, the proposed diplexer can achieve a miniaturized size compared with those from [4,5,10,12] and [15]. As shown in the Table 1, the measured isolation of the proposed design is comparable to other previous designs even through our designed Fractional Bands are much larger. And our design can also achieve very low insertion loss in the wide operation bands compared to other previous designs. It is worth mentioning that the quoted on-chip diplexer designs occupy a large area in the mm-operating band, while this proposed design has more advantages in the 3G, 4G, Wi-Fi and 5G bands and some specific RF systems.

4. Conclusions

A low-loss diplexer with structures of stacked 2D and 3D inductors has been introduced using 3D glass-based advanced packaging technology. By analyzing the coupling effect of the stacked 2D and 3D inductors, the proposed diplexer can achieve low loss and small size simultaneously. The proposed diplexer can achieve an insertion loss less than 0.8 dB and 0.9 dB and an isolation better than 20 dB and 17.5 dB in the bands of 0.699 GHz-0.960 GHz and 1.71 GHz-2.69 GHz, respectively. The size of the proposed diplexer is 1.6 mm × 0.8 mm × 0.25 mm. All the advantages have shown that this design has great application prospect in 3G, 4G, Wi-Fi and 5G bands and also some specific Antenna transceiver in RF systems.

CRediT authorship contribution statement

Qi Zhang: Writing – original draft, Conceptualization. **Yazi Cao:** Writing – review & editing, Writing – original draft, Conceptualization. **Gaofeng Wang:** Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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